

## Description

MOSFET circuit having reduced output voltage oscillations  
5 during a switch-off operation

The present invention relates to a MOSFET circuit having  
reduced output voltage oscillations during a switch-off  
operation during which the current flowing through the  
10 circuit falls to zero.

In SMPSSs (SMPS = Switched Mode Power Semiconductor or  
switched mode power supply) with MOSFETs, the switch-off  
thereof gives rise to high-frequency output oscillations  
15 which bring about interference and thus adversely affect the  
interference spectrum. This applies in particular to SMPSSs  
which use compensation components, namely so-called  
CoolMOS-FETs, as MOSFETs.

20 Compared with SMPSSs with CoolMOS-FETs, corresponding circuits  
with IGBTs are distinguished by a lower-interference  
switching behavior in which significantly fewer high-  
frequency output oscillations arise during switch-off.

25 Figure 4 shows a MOSFET T, which is located with its source-  
gate path and a load L in series between a voltage source +U  
and a reference-ground potential and is driven at its gate G.  
If this MOSFET T is switched off at an instant  $t_0$ , then a  
current I through the MOSFET falls steeply, while an output  
30 voltage  $U_{out}$  rises suddenly and exhibits high-frequency  
output oscillations especially in the case of a CoolMOS-FET,  
as is illustrated in figure 5.

By contrast, during switch-off an IGBT used instead of the  
35 MOSFET T supplies a so-called tail current  $I_{tail}$ , which  
delays the fall in the current I after switch-off at the  
instant  $t_0$  and thus attenuates output oscillations of the

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output voltage  $U_{out}$ , so that the interference spectrum is adversely affected to a lesser extent in comparison with a CoolMOS-FET (cf. figure 6).

5 It is an object of the present invention to provide a MOSFET circuit, in particular for a switched mode power supply, which is distinguished by reduced output voltage oscillations during a switch-off operation, which is also intended to hold true when CoolMOS-FETs are used for the MOSFET circuit.

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This object is achieved according to the invention by means of a MOSFET circuit having the following:

- a first MOS transistor having a first number of cells,

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- a second MOS transistor having a second number of cells, the second number being less than the first number and the second MOS transistor being provided with its source-drain path in parallel with the source-drain path of the first MOS transistor between a voltage source and reference-ground potential, and

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- a constant voltage element between gate of the first MOS transistor and gate of the second MOS transistor.

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A zener diode may advantageously be used for the constant voltage element. A first resistor may be provided in parallel with said zener diode, so that a parallel circuit formed by the zener diode and the first resistor is present.

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A second resistor may be arranged in series with the parallel circuit formed by the constant voltage element or the zener diode and the first resistor.

35 The zener diode and the first resistor may advantageously be integrated with one another. This may be done for example by

the zener diode and the first resistor being formed by a highly doped polycrystalline layer of the first conduction type and a polycrystalline layer of the second conduction type that is in contact with the latter. In this case, the  
5 polycrystalline layer of the second conduction type may be located on the polysilicon gate plane of the MOSFET circuit.

Polycrystalline silicon on the polysilicon gate plane may likewise be used for the second resistor.

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The first and second MOS transistors may advantageously be integrated into a chip or semiconductor body. Silicon, silicon carbide, compound semiconductor or another suitable semiconductor material may be used for the semiconductor  
15 body.

The doping concentration in the highly doped polycrystalline layer forming the zener diode and the first resistor and also in the polycrystalline layer of the second conduction type  
20 should not be higher than  $10^{19}$  charge carriers  $\text{cm}^{-3}$  in order in any event to avoid a short circuit.

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The MOSFET circuit according to the invention is realized in a particularly advantageous manner with CoolMOS-FETs, since  
25 the reduction of the output voltages has a particularly advantageous effect therein.

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The invention is explained in more detail below with reference to the drawings, in which:

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figure 1 shows a schematic circuit diagram of the MOSFET circuit according to the invention,

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figure 2 shows the profile of the current/voltage characteristic curve of a zener diode in the case of the MOSFET circuit according to the invention,

figure 3 shows a schematic sectional illustration through two transistor cells with a realization possibility for a zener diode,

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figure 4 shows a schematic circuit diagram with a CoolMOS-FET,

figure 5 shows a diagram for elucidating the switch-off behavior in the case of a MOSFET, and

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figure 6 shows a diagram for elucidating the switch-off behavior in the case of an IGBT.

15 Figures 4 to 6 have already been explained in the introduction.

In the figures, the same reference symbols are in each case used for mutually corresponding structural parts.

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Figure 1 shows an exemplary embodiment of the MOSFET circuit according to the invention with a first, "larger" MOS transistor T1 and a second, "smaller" MOS transistor T2. In this case, "larger" and "smaller" are to be understood such that the first MOS transistor T1 has more cells than the second MOS transistor T2. In this case, the first MOS transistor T1 may have more cells than the second MOS transistor T2 by a factor of 10, for example. However, it is also possible to provide only the value 2 or less or a value of more than 10 for said factor. By way of example, the transistor T1 may have 1000 cells. The transistor T2 may then be provided with about 100 cells.

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The two MOS transistors T1 and T2 are located with their source-drain paths in parallel with one another between a voltage source +U and a reference-ground potential or ground.

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A load L may additionally be provided between the parallel circuit formed by the two transistors T1 and T2 and the voltage source +U.

5 A control terminal St is connected to gate of the first MOS transistor T1 and, via a resistor R1 and the parallel circuit formed by a zener diode Z1 and a resistor R2, is connected to gate of the second MOS transistor T2. The resistor R1 may have a very low resistance and, if appropriate, also be  
10 omitted. Only the parallel circuit formed by the zener diode Z1 and the resistor R2 is then located between the control terminal St and gate of the MOS transistor T2.

The MOS transistors T1 and T2 are n-channel MOS transistors,  
15 for example, which, in particular, are preferably embodied using compensation technology. Thus, CoolMOS transistors are preferably used here.

If the two transistors T1 and T2 are both in the on state,  
20 then a current I flows from the voltage source +U via the load L and the parallel circuits of the two transistors T1 and T2 to reference-ground potential. In this case, these two transistors T1 and T2 are switched on practically simultaneously by a corresponding signal being applied to the  
25 control terminal St.

If the two transistors T1 and T2 are then switched off at an instant  $t_0$ , the gate voltage drop at the transistor T2 is delayed by a certain time duration until after the gate  
30 voltage drop at the transistor T1, since the zener voltage of the zener diode Z1 is still present momentarily at the gate of the transistor T2. This means that the switch-off of the transistor T2 is delayed with respect to the switch-off of the transistor T1. A "tail current" thus continues to flow  
35 momentarily, so that a switch-off behavior corresponding to

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figure 6 for an IGBT is present for the MOSFET circuit of figure 1.

Instead of the zener diode Z1, it is also possible to use a  
5 different constant voltage element provided that the latter has a characteristic curve as is illustrated for example in figure 2 for the current I as a function of the voltage u across the zener diode Z1.

10 The two transistors T1 and T2 are expediently integrated in a semiconductor body or on a chip. It is then advantageous also to integrate the resistor R1, the resistor R2 and the zener diode Z1 in the same semiconductor body or chip.

15 One exemplary embodiment for this is shown in figure 3. It should be noted in this respect that the conduction types specified may in each case be reversed. Equally, instead of silicon, as has already been mentioned above, it is also possible to use another suitable semiconductor material.

20 Situated in a silicon body 1 with an  $n^+$ -conducting layer 2 and an n-conducting layer 3 there are p-conducting body regions 4, 5, in which respective  $n^+$ -conducting source zones 6, 7 and  $p^+$ -conducting body terminal regions 8, 9 are  
25 incorporated. Source metallizations 10, 11 made of aluminum, for example, are connected to the source zone 6 and, via the body terminal region 8, to the body region 4 and, respectively, to the source zone 7 and, via the body terminal region 9, to the body region 5.

30 The metallizations 10, 11 are essentially situated on an insulating layer 12 made of silicon dioxide, for example, in which gate electrodes 13 made of  $n^+$ -doped polycrystalline silicon are incorporated. One of said electrodes 13 may have  
35 a  $p^+$ -doped polycrystalline region 14, which thus forms a  $p^+/n^+$  diode with zener-like behavior, that is to say the zener

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diode Z1. In this case, the pn junction between the region 14 and the region 13 constitutes the resistor R2.

5 The zener diode with resistor R2 formed by the regions 13, 14 is provided with a metallization 15.

10 The metallizations 10, 11 are introduced into the insulating layer 12 via first contact holes KL1, while the metallization 15 leads to the region 14 via second contact holes KL2 in the insulating layer 12.

15 It is also possible for p-doped compensation regions 16 to be embedded in the layer 3, which may provide for charge compensation in the drift path of the transistors and be floating or nonfloating.

20 Figure 3 shows two cells of a transistor T1 or T2. Each of said transistors may have a multiplicity of such cells, zener diodes (cf. reference symbols 15, 14) only being incorporated in the cells of the transistor T2.

25 Since the MOS transistors T1 and T2 each have cells with an identical construction, for example corresponding to the diagram of figure 3, the MOS transistors T1 and T2 may readily be integrated in a single semiconductor body.

The resistor R1 may readily be realized by polycrystalline silicon on the insulating layer 11.

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List of reference symbols

	T1, T2	MOS transistor
5	R1, R2	Resistor
	Z1	Zener diode
	St	Control terminal
	U, u	Voltage
	I, i	Current
10	L	Load
	Uout	Output voltage
	t0	Instant
	Itail	Tail current
	1	Semiconductor body
15	2	Semiconductor layer
	3	Semiconductor layer
	4, 5	Body region
	6, 7	Source zone
	8, 9	Body terminal region
20	10, 11	Source metallization
	12	Insulating layer
	13	Gate electrode
	14	p <sup>+</sup> -conducting region
	15	Metallization
25	KL1, KL2	Contact hole
	G	Gate
	T	Transistor